Planar hybrid superlattices by compression of rolled-up nanomembranes

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Hybrid metal/semiconductor superlattices are obtained by the controlled compression of rolled-up metal/semiconductor nanomembranes. The planar superlattice maintains the crystalline quality of the semiconductor and the polycrystalline texture of the metal, allowing the integration of these materials into a multilayer system that cannot be produced by any direct deposition procedure. The superlattice consists of two symmetrically inverted multilayer stacks splitted by a metallic mirror plane. Additional intensity peaks in x-ray reflectivity confirm the periodic structure created by the roll up and compression of nanomembranes. © 2009 American Institute of Physics.

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Since the first proposal of superlattices (SLs) for the realization of minibands in semiconductor,¹ such heterostructures have attracted overwhelming interest over the past 30 years due to their electronic, optical, or optoelectronic properties (for a review see, e.g., Ref. 2). Modern growth techniques such as molecular beam epitaxy (MBE) or chemical vapor deposition allow the fabrication of SLs with high quality from various material classes such as semiconductors, oxides, and metals. Combinations of these material classes into SLs have been suggested theoretically³ as suitable structures for spintronics⁴ and thermoelectric devices.⁵

However, combinations of chemically incompatible materials or even material phases (such as single crystalline and amorphous) cannot be grown on substrate surfaces. For this reason, nanomembranes of different materials have been detached from their host substrates and transferred to a target substrate, where they form a stack of hybrid heterostructures.⁶ ⁷ The thickness of transferred nanomembranes is large, though, in the range >200 nm, and SL effects due to, e.g., electronic interactions are not expected in these dimensions.

An alternative approach to create hybrid SLs⁸ ⁹ with periodicities of only a few nanometers is to roll up ultrathin hybrid nanomembranes into a cylindrical geometry on a substrate surface.¹⁰ ¹¹ Still, it might be desirable to have such hybrid structures in a planar geometry for easy integration in aspiring fields such as magnetoelectronics and thermoelectrics.

In this letter, we fabricate a planar metal/semiconductor SL (MeSSL) consisting of a periodic sequence of metal layers of Ti/Au or Cr and III-V semiconductor layers. After the formation of a radial SL (RLS) by the roll up of the metal/semiconductor stack, the RLSs are pressed with a nanoimprinter and transformed into a planar SL. The MeSSL is investigated by transmission electron microscopy (TEM), energy-dispersive x-ray spectroscopy (EDX), and x-ray reflectometry (XRR) in order to clarify the structure of interfaces.

Two types of MeSSLs were produced from layer stacks of Au(40 nm)/Ti(10 nm)/In₀.₂₀Ga₀.₈₀As(20 nm) and Cr(6 nm)/GaAs(3 nm)/In₀.₃₃Ga₀.₆₇As(3 nm), grown on top of 20 nm thick AlAs sacrificial layer on GaAs (001) substrates. The InₓGa₁₋ₓAs and AlAs layers were grown by MBE while the metal layers were deposited by thermal evaporation. For subsequent release of the layers, starting edges were defined by mechanical scratching prior to the removal of the sacrificial layer by diluted HF (c = 2.5%) and roll up of the flat layer stack into a RSL. The rolled-up tube is schematically illustrated in Fig. 1(a) for a Cr/GaAs/InGaAs RSL with a diameter of 1.3 µm [see Fig. 1(b)]. Figure 1(c) shows a representative scanning electron microscopy (SEM) image of a compressed RSL.

To transform the RSL into a planar MeSSL, the samples were placed on a piece of silicon coated with an antisticking layer¹² both loaded in a nanoimprinter from OBUDC. A pressure of 20 bar was applied for 10 min at a temperature of 200 °C. During pressing, the RSL is heated up, and the opposing tube sidewalls touch each other and form permanent bonds. In this way, a compact planar SL is built with a mirror plane in the middle, leading to a phase flip in the periodicity of 180°. A SEM image of the pressed structure is shown in

![Image](https://via.placeholder.com/150)

**FIG. 1.** (Color online) [(a) and (c)] Schematic illustration of the RSL and MeSSL formation by rolling up a metal/semiconductor stack and subsequent pressing. (b) and (d) show SEM images of RSL and MeSSL with a few turns.

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The MeSSL occupies an area of about 1.75 \times 90 \, \mu m^2, elongated along the original tube axis, and a total number of layers defined by the number of turns of the tube walls.

To study the interface and layer quality inside MeSSLs, cross sections of the samples were prepared by focused ion beam (FIB) technique. Scanning TEM (STEM) for both MeSSLs and TEM for the Cr/GaAs/InGaAs MeSSL (hereafter referred as Cr-MeSSL) was carried out in a Zeiss NVision equipped with a STEM detector and in a FEI Tecnei TEM 200 kV, respectively. Chemical analysis was conducted using EDX in the STEM mode of the TEM for the Cr-MeSSL. XRR measurements were performed at the ESRF ID01 beamline. A focused beam with 0.75 \, \mu m vertical and 3 \, \mu m horizontal size was obtained using Be compound refractive lenses. The energy was fixed to 8.5 keV (\lambda = 1.459 \, \text{Å}) using a channel-cut Si (111) monochromator. The system was optimized for third harmonic suppression and lower beam divergence and an avalanche photodiode was used as point detector.

Figure 2(a) displays a STEM image of a FIB prepared cross section of an InGaAs/Ti/Au MeSSL. The upper part of the multilayer is embedded into carbon as a protection layer, deposited for the cross section preparation of a lamella, which includes part of the substrate below the contact point of the pressed tube. The material contrast between the poly-crystalline metal (dark) and the single-crystalline semiconductor (bright) is due to their different atomic number and the crystalline phase is easily observed. The mirror plane formed by a double metal layer leading to two inverted multilayer stacks is clearly visible in the inset of Fig. 2(a). In Fig. 2(b), a magnified TEM image of the cross section of the Cr-MeSSL is shown. Below the SL, the AlAs of the sacrificial layer and the etch stop as well as the start edge of the detached layer can be recognized. The applied pressure occasionally breaks windings, preferentially in the middle of the tube and at the edges, but Fig. 2 demonstrates that the overall number of cracks is small compared to the lateral tube dimensions.

Figures 3(a) and 3(b) display high magnification images of the layer sequence of the Cr-MeSSL [area marked in Fig. 2(b)]. The Cr-MeSSL of Fig. 3(a) consists of 24 periods created by 12 rotations performed by the Cr/GaAs/InGaAs tube. The lower half of the Cr-MeSSL as well as the mirror plane are shown, where the layer sequence inside one period of the MeSSL reverses. This reversal is inherent to the structure due to the inner metal layer in the RSL. The layer sequence of Cr–CrO–CrO–Cr forming the mirror plane is twice as thick (12 nm) as the deposited Cr layer.

A chemical analysis across the lower half of the MeSSL was carried out in Fig. 3(c). The spectra of Cr, O, Ga, and As obtained by the EDX linescan are plotted, and the yellow dashed box in the middle marks the length of one single period. As expected, the intensity maxima of Ga and As coincide at a position where the Cr intensity has a minimum. The linescan covers eight periods of the MeSSL showing the same layer thickness for all periods. The mirror plane is indicated by a light blue box on the right side. Apart from Ga, As, and Cr, oxygen was also monitored during the EDX linescan. The oxygen signal shows broad maxima at a position where the chromium signal has maximum intensity, indicating the existence of oxidized chromium. Moreover the maximum overlaps with the signal of Ga and As over the full period, thus pointing to the existence of oxidized Ga as well as a mixture of Cr, Ga, and O as reported previously.

In order to pinpoint the origin of the oxide signal, a more detailed investigation of the layer sequence is performed in Fig. 3(b). Apart from the metal and the semiconductor bilayer (marked with SC), two thin regions are labeled with IF1 and IF2. These regions represent the interface between two adjacent windings (IF1) and the GaAs/Cr growth interface (IF2). The thickness of the semiconductor bilayer is 7 nm, which is in good agreement with the nominal layer
thickness (6 nm). The metal layer is slightly thinner (4 nm) than the nominal thickness (6 nm). By adding the thickness of the two interfaces (IF1 and IF2) to that of the metal layer, we find the expected Cr layer thickness. We assign the thinning of the metal to the formation of the interface layers IF1 and IF2 during metal deposition, rolling, and pressing. IF1 is the oxidized Cr obtained after evaporation and the subsequent exposure to air, whereas IF2 represents oxidized GaAs formed during the exposure of the wafer after unloading it from the ultra high vacuum. Our results indicate that pressing slightly enlarges IF1 between two succeeding windings of the rolled-up tube. This might be explained by the heat and pressure-mediated diffusion of the oxide into adjacent layers as well as additional oxidation during pressing. Moreover, due to the heat of the vapor beam during thermal evaporation, chemical reactions with the underlying oxidized GaO (IF2) can form a complex mixture of oxidized GaAs and Cr.

Finally, Fig. 4 shows reflectivity curves recorded at positions marked with color-coded spots along a path illustrated in the lower inset. Starting at a position where the beam mainly illuminates the GaAs surface (black plot), a distinguished peak at $q=0.19$ Å$^{-1}$ arises at the edge of the MeSSL (green plot) and becomes more pronounced when the Cr-MeSSL is centered with respect to the beam (blue). The pink curve shows the data of the reference flat surface, which comprises the reflectivity signal of the unetched Cr/GaAs/InGaAs trilayer and AlAs sacrificial layer. Two rising peaks, one at 0.19 Å$^{-1}$ and the other at 0.24 Å$^{-1}$, are the most pronounced features of the pressed layer system, marked by arrows in Fig. 4. The width of the peak at $q=0.19$ Å$^{-1}$, estimated as $\Delta q=0.007$ Å$^{-1}$ is equivalent to a 90 nm thick layer stack, suggesting a partially coherent interference along one half of the pressed Cr-MeSSL. Even though a distinct rise of certain peaks can be observed, no clear periodic multilayer oscillations are present in the XRR curve. This indicates that the MeSSL forms a stack of layers but a partial loss of phase coherence over several periods of the multilayer takes place. This can either arise from the observed oxide formation at the interfaces or, most likely, due to small thickness fluctuations of the Cr/GaAs/InGaAs walls caused by pressing faults and voids along the MeSSL layers. Since the x-ray beam spans laterally over 3 μm, many of these small voids are illuminated, as well as parts of the flat etched and unetched areas, preventing a coherent summation of the layer-to-layer reflectivity signal and making a fit of the reflectivity curves too complex to the scope of this work. Such variations on the wall matching quality are observed in the TEM images, e.g., in Fig. 3(a). Detection of a weak tube signal (or signal from the initial bilayer) in areas next to the compressed tube are caused by the large illuminated area resulting from the shallow incident angle and the finite tube size.

In conclusion, we have fabricated a planar hybrid SL by pressing a RSL of Au/Ti/InGaAs and Cr/GaAs/InGaAs into a multifold stack consisting of polycrystalline metal and single crystalline semiconductor. The MeSSls consist of two symmetric SLs, mirrored in the middle of the structure. Chemical analysis by EDX confirmed the periodicity of the layers as well as the existence of oxidized Cr and GaAs interface layers. XRR was applied to reveal the chemical contrast and a partially coherent phase superposition of the MESSL.

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