Characteristics of polycrystalline silicon Schottky barrier thin film transistors fabricated using metallic junction source/drain with erbium silicide and platinum silicide

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(Received 11 September 2008; accepted 24 December 2008; published online 3 February 2009)

Polycrystalline silicon (poly-Si) Schottky barrier thin film transistors (SB-TFTs) were fabricated using platinum and erbium silicided source/drain for p- and n-channel SB-TFTs, respectively. High quality poly-Si films were obtained by crystallizing the amorphous Si films with the excimer laser annealing method. Poly-Si SB-TFTs with metallic source/drain junctions showed a large on/off current ratio and a low leakage current. Significant improvements in electrical characteristics were obtained by additional forming gas annealing in 2% H2/N2 gas ambient due to the termination of dangling bonds at the grain boundaries of the poly-Si film as well as the reduction in interface trap states at gate oxide/poly-Si channel. © 2009 American Institute of Physics.

DOI: 10.1063/1.3073047

Metal-oxide-semiconductor field effect transistors (MOSFETs) with conventional materials and structures have been extended to the performance limitations.1 For the further scale down of MOSFETs, an intensive study regarding high-K gate insulators, strained-silicon substrates, metal gate, and metallic junction source/drain (S/D) is necessary.2,3 Schottky barrier (SB) MOSFETs replacing the impurity doped junction with metallic junction for S/D have numerous advantages such as a simple process for S/D formation, low parasitic S/D resistance, strong short channel effect immunity, and inherent physical scalability to sub-100 nm gate length.4–6 Also, SB-MOSFET technologies allow for the use of high-K materials and metal gates in high performance electronic devices due to a low temperature processing for S/D formation.7 In this study, the poly-Si TFTs with metallic S/D junctions were investigated to fabricate high performance SB-TFTs for system-on-glass (SOG) application. Although the electrical characteristics of poly-Si films on insulators are inferior to single crystalline bulk silicon or silicon-on-insulator substrate, poly-Si TFTs have great advantages such as a large process area, a stacked device structure, low cost, and the application of display.8,9

p-channel and n-channel poly-Si SB-TFTs were fabricated using a poly-Si film on insulator. Thermal oxide films of 200-nm-thick were grown on (100) p-type bulk silicon wafers with a resistivity of 10–20 Ω cm. The deposition of an amorphous Si film with a thickness of 100 nm was followed by the low pressure chemical vapor deposition method at 530 °C. Then the amorphous Si films were crystallized in a vacuum chamber at 300 mtorr using the KrF excimer laser with a wavelength of 248 nm. The laser beam was homogenized line beam of 1.1×55 mm² size and the pulse duration was 25 ns. The crystallization process temperature during excimer laser annealing (ELA) was maintained at 20 °C and the energy density was changed from 300 to 600 mJ/cm². The poly-Si active region of TFT was defined by photolithography and the plasma reactive ion etching (RIE) process. Then the thermal oxide with a thickness of 5 nm was grown as gate oxide and the phosphorus doped poly-Si with a thickness of 100 nm was deposited as gate electrode. The gate electrode was defined by photolithography and RIE. Particularly the sidewall spacer for preventing an electrical short between the S/D and the gate electrode was formed by the thermal oxidation of poly-Si gate electrode and the plasma etchback of thermally grown oxide. In order to form the metallic junctions, 50-nm-thick Pt and Er layers were deposited by rf magnetron sputter in Ar ambient. For Er-silicide S/D junction formation, a rapid thermal annealing (RTA) at 500 °C for 3 min in 1×10−6 Torr was performed. Meanwhile, a consecutive furnace annealing at 300 °C for 30 min was followed by RTA at 500 °C for 1 min for Pt-silicided S/D junction formation. Nonreactive Er and Pt on the oxide surface were removed by sulfuric acid peroxide mixture (H2SO4:H2O2=1:1) solution and aqua regia solution, respectively. Finally, the poly-Si SB-TFTs were annealed in 2% diluted hydrogen (H2/N2) ambient at 450 °C for 30 min to improve the electrical characteristics.

Figure 1 shows the scanning electron microscope (SEM) images of poly-Si films crystallized by the ELA method. Secco etching was performed before observing the poly-Si surface by SEM to distinguish between silicon grains and grain boundaries.10 It is found that poly-Si films crystallized by ELA with an energy density of 400 and 500 mJ/cm² have large grain. However, the ELA energy density higher than 500 mJ/cm² coarsened the surface of the poly-Si film. Moreover, the grain size decreased and the surface damage increased when the ELA energy density is 600 mJ/cm². From the grain size and surface damage, the optimized energy density of ELA is 400 mJ/cm².

Figure 2 shows the results of x-ray diffraction analysis (XRD) for ELA crystallized poly-Si films. Strong diffraction peaks corresponding to the crystal faces of (111), (220), and

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(311) are observed from all poly-Si films. Among these results, the peaks of XRD for 400 mJ/cm² have strongest intensity. Also, the full width at half maximums (FWHMs) for 300, 400, 500, and 600 mJ/cm² at (111) peak are extracted as 0.3845, 0.35829, 0.3735, and 0.4260, respectively. Since the FWHMs of these values are related to the grain size of poly-Si films, a smaller FWHM value means a larger grain size.11,12 These results coincide well with the SEM images shown in Fig. 1. Therefore, the ELA energy density of poly-Si films, a smaller FWHM value means a larger grain size.

Figure 3 shows the drain current-gate voltage ($I_D$-$V_G$) and the drain current-drain voltage ($I_D$-$V_D$) characteristics of $p$- and $n$-channel SB-TFTs before and after forming gas annealing (FGA). The electrical measurements were performed at room temperature and the channel width/gate length ($W/L$) is 20/20 μm. The sheet resistances of ErSi and PtSi were less than 30 and 10 Ω/□, respectively. For $I_D$-$V_G$ characteristics, the drain voltage ($V_D$) was kept constant at 0.05 and 1 V. Both $p$- and $n$-channel poly-Si SB-TFTs have a high on/off current ratio ($I_{on}/I_{off}$) greater than $10^6$ with low leakage current. In the case of as-silicided SB-TFTs plotted by closed squares, the threshold voltage ($V_t$) was −3.24 V and the subthreshold swing (SS) was 590 mV/decade for $p$-channel SB-TFTs. In the case of as-silicided $n$-channel SB-TFTs, the $V_t$ and SS were 1.1 V and 207 mV/decade, respectively. On the other hand, the FGA in a 2% diluted hydrogen ($H_2/N_2$) ambient significantly improved the electrical characteristics of poly-Si SB-TFTs as plotted by open circles; $V_t$=−2.3 V and SS=304 mV/decade for the $p$-channel and $V_t$=0.61 V and SS=144 mV/decade for the $n$-channel. As shown in Fig. 3(b), the drain current also increased with FGA treatment. Compared with these results, previous works reported poor performances of SB-TFTs with a low on/off current ratio and a large SS by using several silicide materials; CoSi, NiSi, YSi, and DySi$_2$.13–16 The on/off current ratios of previous works range from $10^2$ to $10^3$ and the SS range from 450 to 1500 mV/decade. This insufficient performance could be attributed to large SB height and the distribution of trap states at the grain boundaries and interfaces. On the other hand, the ErSi and PtSi used in this work have low SB heights for electrons and holes. Therefore, the improvement of electrical characteristics of SB-TFTs by FGA treatment is considered attributable to the termination of the dangling bonds at the grain boundaries of the poly-Si film and the reduction trap states at the interface of gate oxide/poly-Si channel and at the interface of metal silicide/poly-Si channel.
In summary, the electrical characteristics of $p$- and $n$-channel poly-Si SB-TFTs were investigated. To obtain high quality poly-Si films, amorphous-Si films were crystallized by the ELA method. The energy density with a 400 mJ/cm$^2$ was the optimum condition for large grain size and low surface damage. The metallic junctions for S/D were formed using PtSi and ErSi for $p$-channel and $n$-channel SB-TFTs, respectively. The fabricated poly-Si SB-TFTs showed a high on/off current ratio and low leakage current. The electrical characteristics were significantly improved by FGA treatment due to the reduction in interface trap states distributed at the grain boundaries of the poly-Si channel at the interface of gate oxide/poly-Si channel and at the interface of metal silicide/poly-Si channel. These results suggest that the SB-TFTs with ErSi and PtSi at S/D regions are promising devices for the SOG applications.

This work was supported by the Korea Research Foundation Grant funded by the Korean Government (MOEHRD, Basic Research Promotion Fund) (Grant No. KRF-2007-331-D00253).