Dependence of charge trapping and tunneling on the silicon-nitride (Si$_3$N$_4$) thickness for tunnel barrier engineered nonvolatile memory applications

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Charge trapping and tunneling characteristics of silicon-nitride (Si$_3$N$_4$) layer with various thicknesses were investigated for applications of tunnel barrier engineered nonvolatile memory (NVM). A critical thickness of Si$_3$N$_4$ layer for suppressing the charge trapping and enhancing the tunneling sensitivity of tunnel barrier were developed. Also, the charge trap centroid and charge trap density were extracted by constant current stress method. As a result, the optimization of Si$_3$N$_4$ thickness considerably improved the performances of NVM. DOI: 10.1063/1.3078279

Floating gate-type flash memory devices are rapidly approaching the limit of scaling associated with floating gate coupling and gate leakage current, while the charge trap flash (CTF)-type memory devices have attracted much attention due to their advantages over traditional floating gate-type flash memory devices, such as lower programming voltage, better scalability, improved endurance, and a simple fabrication process compatible with standard complementary metal-oxide semiconductor technology. Moreover, the fabrication process compatible with standard complementary metal-oxide semiconductor technology.2,3 Moreover, the CTF-type devices have fundamental problems with a trade-off between the data erasing speed and the data retention time. When the tunnel oxide is thin, the program and erase process become faster but a charge leakage decreases the retention time. On the other hand, when the tunnel oxide is thick, a long charge retention time can be achieved but a higher voltage and a longer time are required to program and erase. In order to overcome these problems, the NVM using the engineered tunnel barriers with high-k/low-k stacks were proposed as one of the solutions for improving the device performances.6–9 Engineered tunneling barriers suppress the direct tunneling at low electric field region during retention operation due to the increase in physical oxide thickness, while it allows efficient tunneling of electrons and holes at a high electric field region due to the band offset and enhanced field sensitivity.10,11 The trapping and tunneling characteristics of Si$_3$N$_4$ and SiO$_2$ layers have been extensively studied for logic applications.12–14 Also, the NVM devices with high-k materials as charge trapping layer have been reported by several groups.15,16 Nevertheless, the characteristics of charge trapping and tunneling of high-k materials are not well understood for NVM applications.

In this paper, the charge trapping and tunneling characteristics of Si$_3$N$_4$ as a high-k layer were studied. The metal-nitride-oxide-semiconductor (MNOS) capacitors with various thicknesses of Si$_3$N$_4$ layer were fabricated, and the critical thickness of Si$_3$N$_4$ layer was developed from the electrical characteristics for the applications of tunnel barrier to the NVM.

MNOS memory devices were fabricated on the Si (100) wafers of both n- and p-type with resistivity of 1–10 $\Omega$ cm as the starting substrates. The surface of Si wafer was cleaned in sulfuric peroxide mixture (H$_2$SO$_4$:H$_2$O$_2$=1:1) solution for 10 min and a chemical oxide was etched in diluted HF (H$_2$O:HF=30:1) for 10 s. After a growth of thermal oxide with a thickness of 2 nm at 700 °C in dry O$_2$ ambient, a deposition of Si$_3$N$_4$ layers range from 6.7 to 2 nm was followed by low pressure chemical vapor deposition at 720 °C to evaluate the thickness effect on the charge trapping and tunneling characteristics. The thickness of deposited Si$_3$N$_4$ layers was measured by spectroscopic ellipsometer and transmission electron microscopy (TEM).

Figure 1 shows the TEM images of Si$_3$N$_4$/SiO$_2$ layers on Si substrates. After the formation of tunneling dielectric layers, the Al layer of 150 nm thick was deposited by electron beam evaporator. The Al gate electrode with a rectangular shape of $310 \times 230 \mu m^2$ area was formed by photolithography. Finally, the current-voltage (I-V), capacitance-voltage (C-V), and constant current stress (CCS) measurements were carried out using HP-4156B semiconductor parameter analyzer and HP-4284A LCR meter.

Figure 2 shows the tunneling current characteristics of MNOS memory devices with various thicknesses of Si$_3$N$_4$ layer. The 6.7-nm-thick Si$_3$N$_4$ layer shows the lowest gate current density. The tunneling current was almost the same...
with decrease in Si$_3$N$_4$ thickness from 6.7 to 5 nm. However, a significant increase in tunneling current was observed as reducing the thickness of Si$_3$N$_4$ layer from 5 to 4 nm. This means that the tunneling of electron is significantly changed with decrease in Si$_3$N$_4$ thickness from 5 to 4 nm. This result implies that there is little charge trapping in Si$_3$N$_4$ layers below the thickness of 4 nm. This result is consistent with results of $I$-$V$ measurements. To understand the dependence of charge trapping and tunneling characteristics on the thickness of Si$_3$N$_4$ layer, the charge trap centroid ($X_{\text{cent}}$) and charge trap density ($C_{\text{trap}}$) were evaluated by using the CCS measurement. The $X_{\text{cent}}$ and $C_{\text{trap}}$ in insulating layers are given by

$$X_{\text{cent}} = \frac{t_{\text{stack}}}{[1 - (\Delta V_g^+ / \Delta V_g^-)],}$$

$$C_{\text{trap}} = \frac{\varepsilon_0 e_{\text{stack}}}{t_{\text{stack}}} \left(1 - \Delta V_g^- / \Delta V_g^-\right),$$

where $X_{\text{cent}}$ is measured from the metal gate/oxide interface, and $\Delta V_g^+$ and $\Delta V_g^-$ are the negative and positive gate voltage shifts, respectively. The extracted values of $X_{\text{cent}}$ and $C_{\text{trap}} / C_{\text{total}}$ are shown in Table I. The charge trap centroid ($X_{\text{cent}}$) shifts to the gate/oxide interface as the thickness of Si$_3$N$_4$ layer decreases. Especially, in case of 4-nm-thick Si$_3$N$_4$ layer, the $X_{\text{cent}}$ (3.33 nm) is very close to the Si$_3$N$_4$/SiO$_2$ interface. Therefore, the dominant charge trap changes from the bulk traps in Si$_3$N$_4$ layer to the interface states at Si$_3$N$_4$/SiO$_2$. Furthermore, the trapping efficiency defined as the ratio of trapped charges to total injected charges ($C_{\text{trap}} / C_{\text{total}}$) considerably decreased from 2.96% to

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<th>Table I. Extracted trapping parameters of MNOS capacitors with various thicknesses of Si$_3$N$_4$.</th>
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<td>$T_{\text{SiO}_2/\text{Si}_3\text{N}_4}$</td>
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<td>2/6.7</td>
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0.16% as the thickness of Si$_3$N$_4$ layer decreased from 5 to 4 nm. Meanwhile, the change in $C_{\text{trap}}/C_{\text{total}}$ in thicker Si$_3$N$_4$ layer is small: 3.68% for 6.7 nm and 2.96% for 5 nm. Therefore, it is considered that a rapid increase in tunneling current and a decrease in memory windows for the Si$_3$N$_4$ layer thinner than 4 nm are attributable to the reduction in charge trapping characteristics. Consequently, for the tunnel barrier application of NVM, the thickness of Si$_3$N$_4$ layer should be thinner than 4 nm. On the other hand, for the charge storage application, the thickness of Si$_3$N$_4$ layer thicker than 5 nm is necessary.

In summary, the charge trapping and tunneling characteristics of MNOS memory with various thicknesses of Si$_3$N$_4$ layer were investigated. We confirmed that a significant increase in tunneling current and no charge trapping characteristic under 4-nm-thick Si$_3$N$_4$ layer. These results were explained by the shift in charge trap centroid as the thickness of Si$_3$N$_4$ layer decreases. For thin Si$_3$N$_4$ layer less than 4 nm thick, the position of charge trap centroid is very close to the Si$_3$N$_4$/SiO$_2$ interface. As a result, the tunneling current rapidly increases and the memory windows decrease for thin Si$_3$N$_4$ layer. Finally, these results would provide advantages in stacked tunnel barrier layers and charge storage, which is critical issue for next generation NVM devices. For the tunnel barrier application of NVM, the thickness of Si$_3$N$_4$ layer should be thinner than 4 nm. On the other hand, for the charge storage application, the thickness of Si$_3$N$_4$ layer thicker than 5 nm is required.

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